WBGlobalSemi, Inc.

High Power Design System Data Sheet 8/1/19

Our design goals are fastest switching for current & future WBG power devices, while minimizing overvoltages, inadvertent faults, and other switching issues.

High Power Design System (HPDS):

Power Module with Commercial 3.3 kV, 50 A SiC MOSFET & gate drive

Universal Gate Drive Architecture with Enhanced Protection (UGDA)

Fast Switching – critically damped gate output switching without ringing

Includes CF, CMTI Filter Circuit to Accommodate dV/dt output switching noise to 1000V/ns

Enhanced Fault Protection – for overcurrent, overvoltage, over temperature with low latency fault feedback

Our goals for high Voltage applications include faster switching, greater dV/dt CMTI noise tolerance, and greater protection.

(1) High speed desaturation/overcurrent event shut down protection with turnoff in < 500 ns

(2) Safely withstand dV/dt switching noise from > 200 V/ns to 1,000 V/ns.

(3) Higher speed switching of SiC MOSFETs for extracting greater efficiency and reliability.

For example our overcurrent comparator's output, VFBAR will provide overcurrent error output back to the controller < 20ns max from the PM. This feature allows power control techniques such as adaptive dead time control for high power - to potentially reduce power loss by 12% in voltage mode converters.

Phase 1 Technical Goals of Universal Gate Driver Amplifier With SiC MOSFET (50A 3.3KV) and Desaturation/Overcurrent Protection					
Parameter	**Conditions** (Unless Otherwise, V_{HCC}=20V, $-V_{EE}$=-5V)	**Min**	**Typ**	**Max**	**Units**
Common Mode Transient Immunity, CMTI	CF, CMTI Filter, dV/dt Noise Filter Circuit Inserted	500	1000	2000	V/ns
Switching Frequency Range, f_{sw}		1		200	Khz
Input to Ouptut Delays, t_d			50	70	ns
Rise Time, t_r	Gate Drive Amplifier Driving C_{LD}=4nF, R2=2Ω			20	ns
Fall Time, t_f				20	ns
Desaturation/Overcurrent Detection Threshold, V_{DSTH}	Internally Programmable		10		V
Diode Clamp Voltage Set, V_{DSAT}	Internally Programmable		18		V
Overcurrent Comparator Delay, V_{Fbar}	From the Time when $\|V_{DSAT}-V_{DSTH}\| > \|5mV\|$			20	ns
Overcurrent "Softly" Shutdown	Externally Adjustable, R3=60Ω		400		ns
Overcurrent Blanking	Internally Programmable	100	400		ns

Sam Ochi, MSEE, WBGS VP Engineering, designed 35 gate drives and 100+ commercial analog, digital, mixed signal, and power semiconductors working at National Semi, AMD, Teledyne, Maxim, IXYS, Analog Devices, and Microsemi (now Microchip).